CLAIMS

What is claimed is:

1. A power amplifier of a type comprising at least a load element and at least an active element inserted, in series to each other, between a first and a second voltage reference, wherein said load element includes a DMOS transistor.

2. The power amplifier according to claim 1 wherein said active element comprises a VLSI CMOS transistor.

3. The power amplifier according to claim 1 wherein said active element comprises a high frequency bipolar transistor.

4. The power amplifier according to claim 2 wherein said DMOS transistor is sized and biased so that the VLSI CMOS transistor works in saturation area and complies with a relation:

$$Vx \geq (Vg2 - V_{th2})$$

wherein:

Vx is a voltage value on a terminal of said VLSI CMOS transistor;

Vg2 is a voltage value on a control terminal of said VLSI CMOS transistor; and

Vth2 is a threshold voltage value of said VLSI CMOS transistor.

5. The power amplifier according to claim 1 wherein said load element has a control terminal to receive a first control voltage being set so that the active element works in saturation area.

6. The power amplifier according to claim 1 wherein said active element comprises a resistive element inserted between a circuit node connecting said active element to said load element and said voltage reference.

7. An apparatus, comprising:

a load element having a first terminal coupled to a first voltage reference, a second terminal coupled to receive a first control voltage, and a third terminal; and

an active element in cascode configuration and having a first terminal coupled to the third terminal of the load element, a second terminal coupled to receive a second control voltage, and a third terminal coupled to a second voltage reference,

wherein the second control voltage is set and integration limits of the load element are fixed to allow the active element to operate in a saturation area to provide high cutoff frequency and a high transconductance value and in a linear area to prove low activation resistance.

8. The apparatus of claim 7 wherein the load element comprises a DMOS transistor.

9. The apparatus of claim 7 wherein the active element comprises a VLSI CMOS transistor.

10. The apparatus of claim 7 wherein the active element comprises a bipolar transistor.

11. The apparatus of claim 7, further comprising a resistive element coupled between the third terminal of the load element and the second voltage reference to stabilize a node at the third terminal of the load element.

12. The apparatus of claim 7 wherein the load element and the active element are coupled to provide a high breakdown voltage in the saturation area.

13. A power amplifier usable in radio frequency applications, the power amplifier comprising:

first and second voltage references;

a transistor load element having a first terminal coupled to the first voltage reference, a second terminal coupled to receive a first control voltage, and a third terminal; and

an active element in cascode configuration and having a first terminal coupled to the third terminal of the transistor load element, a second terminal coupled to a second control voltage, and a third terminal coupled to the second voltage reference, wherein the transistor load element is sized and biased and the second control voltage is set to allow the active element to operate in a saturation area to provide high cutoff frequency and a high transconductance value and in a linear area to prove low activation resistance.

14. The power amplifier of claim 13 wherein the transistor load element and the active element are coupled to provide a high breakdown voltage in the saturation area.

15. The power amplifier of claim 13 wherein the transistor load element comprises a DMOS transistor.

16. The power amplifier of claim 13 wherein the active element comprises either a VLSI CMOS transistor or a bipolar transistor.

17. The power amplifier of claim 13, further comprising a resistive element coupled between the third terminal of the transistor load element and the second voltage reference.

18. A method, comprising:

sizing and biasing a transistor load element to allow an active element to operate in a saturation area;

receiving a first control voltage at a control terminal of the load element to allow the active element to operate in the saturation area;

setting a second control voltage at a control terminal of the active element to allow the active element to operate in the saturation area; and

obtaining high cutoff frequencies and high transconductance values in the saturation area, and obtaining low on-state resistance values in a linear area of operation.

19. The method of claim 18, further comprising stabilizing a circuit node between the transistor load element and the active element with a resistive element.

20. The method of claim 18, further comprising obtaining high breakdown voltage values in the saturation area.

21. An apparatus, comprising:

a means for sizing and biasing a transistor load element to allow an active element to operate in a saturation area;

a means for receiving a first control voltage at a control terminal of the load element to allow the active element to operate in the saturation area;

a means for setting a second control voltage at a control terminal of the active element to allow the active element to operate in the saturation area; and

a means for obtaining high cutoff frequencies and high transconductance values in the saturation area, and obtaining low on-state resistance values in a linear area of operation.

22. The apparatus of claim 21, further comprising a means for obtaining high breakdown voltage values in the saturation area.

23. The apparatus of claim 21, further comprising a means for stabilizing a circuit node between the transistor load element and the active element.

24. The apparatus of claim 21 wherein the means for stabilizing the circuit node comprises a resistive element.